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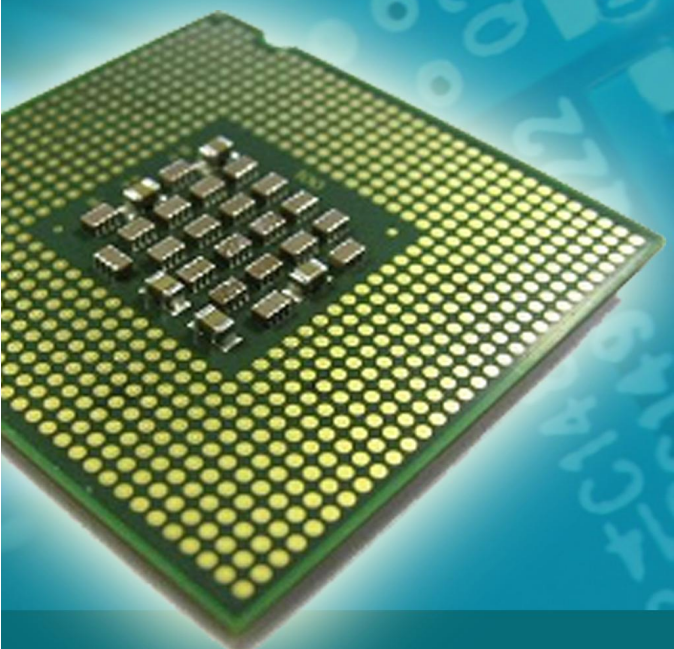
SOLUTIONS PVT LTD

VLSI
PROJECT TITLE
2017 - 2018



VLSI			
S.NO	**PROJECT CODE**	**TITLE**	**YEAR**
ANALOG AMS(TANNER EDA)			
01	ITVL01	20-Mb/s GFSK Modulator Based on 3.6-GHz Hybrid PLL With 3-b DCO Nonlinearity Calibration and Independent Delay Mismatch Control	2017
02	ITVL02	Delay Analysis for Current Mode Threshold Logic Gate Designs	2017
03	ITVL03	CMCS: Current-Mode Clock Synthesis	2017
04	ITVL04	A Closed-Form Expression for Minimum Operating Voltage of CMOS D Flip-Flop	2017
05	ITVL05	Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit	2017
06	ITVL06	A 0.1–2-GHz Quadrature Correction Loop for Digital Multiphase Clock Generation Circuits in 130-nm CMOS	2017
07	ITVL07	12T Memory Cell for Aerospace Applicationsin Nanoscale CMOS Technology	2017
08	ITVL08	Low-Power Variation-Tolerant Non-volatile Lookup Table Design	2016
09	ITVL09	Designing Tunable Sub-threshold Logic Circuits Using Adaptive Feedback Equalization	2016
10	ITVL10	High-Speed, Low-Power, And Highly Reliable Frequency Multiplier For DLL-Basedclock Generator	2016
XILINX SYSTEM GENERATOR			
11	ITVL11	Hardware Implementation Of Polyphone-Decomposition-Based Wavelet Filters For Power System Harmonics Estimation	2017

12	ITVL12	Area/Energy-Efficient Gamma tone Filtersbased On Stochastic Computation	2017
13	ITVL13	FPGA-Based Electrocardiography (ECG) Signal Analysis Systemusing Least-Square Linear Phase Finite Impulse Response (Fir) Filter	2016
14	ITVL14	A Low-Power Broad-Bandwidth Noise CancellationVLSI Circuit Design For In-Ear Headphones	2016
15	ITVL15	Efficient Advance Encryption Standard (AES) Implementation On FPGA Using Xilinx System Generator	2016
DIGITAL SIGNAL PROCESSING			
16	ITVL16	DSP48E Efficient Floating Point Multiplier Architectures On FPGA	2017
17	ITVL17	Low Complexity And Critical Path Based VLSI Architecture For LMS Adaptive Filter Using Distributed Arithmetic	2017
18	ITVL18	Operating Frequency Improvement On FPGA Implementation Of A Pipeline Large-FFT Processor	2017
19	ITVL19	A 4096-Point Radix-4 Memory-Based FFT Using Dsp Slices	2017
20	ITVL20	Multipliers-Driven Perturbation Of Coefficients For Low-Power Operation In Reconfigurable Fir Filters	2017
21	ITVL21	Algorithm And Architecture Design Of Adaptive Filters With Error Nonlinearities	2017
22	ITVL22	Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units	2016
23	ITVL23	A High-Performance Fir Filter Architecture For Fixed And Reconfigurable Applications	2016
24	ITVL24	Approximate Radix-8 Booth Multipliers For Low-Power And High-Performance Operation	2016

25	ITVL25	A New Paradigm Of Common Sub-expression Elimination By Unification Of Addition And Subtraction	2016
DIGITAL DESIGN			
26	ITVL26	Optimal Design Of Reversible Parity Preserving New Full Adder / Full Subtractor	2017
27	ITVL27	Floorplanning Automation forPartial-Reconfigurable FPGAs viaFeasible Placements Generation	2017
28	ITVL28	Design Of Power And Area Efficient Approximate Multipliers	2017
29	ITVL29	Digit-Level Serial-In Parallel-Out Multiplier Using Redundant Representation For A Class Of Finite Fields	2017
30	ITVL30	ROBA Multiplier: A Rounding-Based Approximate Multiplier For High-Speed Yet Energy-Efficient Digital Signal Processing	2017
31	ITVL31	Improved 64-Bit Radix-16 Booth Multiplier Based On Partial Product Array Height Reduction	2017
32	ITVL32	Dual-Quality 4:2 Compressors For Utilizing In Dynamic Accuracy Configurable Multipliers	2017
33	ITVL33	RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder	2017
34	ITVL34	Design and Analysis of Multiplier Using Approximate 15-4 Compressor	2017
35	ITVL35	High-Speed And Energy-Efficient Carry Skip Adder Operating Under A Wide Range Of Supply Voltage Levels	2016
36	ITVL36	A New Fast And Area-Efficient Adder-Based Sign Detector For Rns $\{2n-1, 2n, 2n+1\}$	2016
37	ITVL37	A Fused Floating-Point Four-Term Dot Product Unit	2016

38	ITVL38	Ultralow-Energy Variation-Aware Design: Adder Architecture Study	2016
39	ITVL39	Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation	2016
40	ITVL40	Application-Specific Low-Power Multipliers	2016
FPGA DESIGN			
41	ITVL41	Design Of Efficient Multiplier Less Modified Cosine-Based Comb Decimation Filters: Analysis And Implementation	2017
42	ITVL42	Generating AMS Behavioral Models with Formal Guarantees on Feature Accuracy	2017
43	ITVL43	Compact Implementations of FPGA-Based PUFs with Enhanced Performance	2017
44	ITVL44	High Performance Parallel Decimal Multipliers Using Hybrid BCD Codes	2017
45	ITVL45	HUB-Floating-Point for improving FPGA implementations of DSP Applications	2017
46	ITVL46	A Residue-to-Binary Converter for the Extended Four-Moduli Set $\{2n - 1, 2n + 1, 22n + 1, 22n+p\}$	2017
47	ITVL47	Leveraging Unused Resources for Energy Optimization of FPGA Interconnect	2017
48	ITVL48	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	2017
49	ITVL49	Hybrid LUT/Multiplexer FPGA Logic Architectures	2016
50	ITVL50	FPGA-Based Architecture For A Multisensory Barrier To Enhance Railway Safety	2016
51	ITVL51	On Efficient Retiming of Fixed-Point Circuits	2016
52	ITVL52	Implementation Of AES UsingReversible Cellular Automata BasedS-Box	2016
STATIC TIME ANALYSIS			
53	ITVL53	A Mismatch-Insensitive Skew Compensation Architecture For Clock Synchronization In	2017

		3-D ICS	
54	ITVL54	RSFQ/ERSFQ Cell Library With Improved Circuit Optimization, Timing Verification, And Test Characterization	2017
VLSI WITH MATLAB			
55	ITVL55	High Performance Integer DCT Architectures For HEVC	2017
56	ITVL56	A Scalable Approximate DCT Architectures ForEfficient HEVC Compliant Video Coding	2017
57	ITVL57	LUT Optimization For Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter	2017
58	ITVL58	Multiplierless Unity-Gain SDF-FFTS	2017
59	ITVL59	On Efficient Retiming Of Fixed-Point Circuits	2017
60	ITVL60	Logic Testing with Test-per-Clock Pattern Loadingand Improved Diagnostic Abilities	2017
61	ITVL61	Input-Based Dynamic Reconfiguration Of Approximate Arithmetic Unitsfor Video Encoding	2016
62	ITVL62	Floating-Point Butterfly Architecture Based OnBinary Signed-Digit Representation	2016
63	ITVL63	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable OrthogonalApproximation of DCT	2016
64	ITVL64	$(4 + 2\log n)\Delta G$ Parallel Prefix Modulo-$(2n - 3)$Adder via Double Representationof Residues in [0, 2]	2016
QCA TECHNOLOGY			
65	ITVL65	Design of Efficient BCD Adders in Quantum DotCellular Automata	2017
66	ITVL66	Use: A Universal, Scalable, And Efficientclocking Scheme For QCA	2017

67	ITVL67	Design Of Adder And Subtract or Circuits In majority Logic-Based Field-Coupled QCA nano computing	2017
DESIGN FOR TESTABILITY			
68	ITVL68	Tri-modal Scan-Based Test Paradigm	2017
69	ITVL69	Low-Power Programmable PRPG With Test Compression Capabilities	2016
70	ITVL70	Design for Testability Support for Launch andCapture Power Reduction in Launch-Off-Shiftand Launch-Off-Capture Testing	2016