



FPGA DESIGN			
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249.	ITVL43	Compact Implementations of FPGA-Based PUFs with Enhanced Performance	2017
250.	ITVL44	High Performance Parallel Decimal Multipliers Using Hybrid BCD Codes	2017
251.	ITVL45	HUB-Floating-Point for improving FPGA implementations of DSP Applications	2017
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266.	ITVL62	Floating-Point Butterfly Architecture Based On Binary Signed-Digit Representation	2016
267.	ITVL63	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT	2016
268.	ITVL64	$(4 + 2\log n)\Delta G$ Parallel Prefix Modulo- $(2n - 3)$ Adder via Double Representation of Residues in $[0, 2]$	2016
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271.	ITVL67	Design Of Adder And Subtract or Circuits In majority Logic-Based Field-Coupled QCA nano computing	2017
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272.	ITVL68	Design for Testability Support for Launch and Capture Power Reduction in Launch-Off-Shift and Launch-Off-Capture Testing	2017
272.	ITVL69	Low-Power Programmable PRPG With Test Compression Capabilities	2016

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