



FPGA DESIGN			
247.	ITVL41	Design Of Efficient Multiplier Less Modified Cosine-Based Comb Decimation Filters: Analysis And Implementation	2017
248.	ITVL42	Generating AMS Behavioral Models with Formal Guarantees on Feature Accuracy	2017
249.	ITVL43	Compact Implementations of FPGA-Based PUFs with Enhanced Performance	2017
250.	ITVL44	High Performance Parallel Decimal Multipliers Using Hybrid BCD Codes	2017
251.	ITVL45	HUB-Floating-Point for improving FPGA implementations of DSP Applications	2017
252.	ITVL46	A Residue-to-Binary Converter for the Extended Four-Moduli Set $\{2n - 1, 2n + 1, 22n + 1, 22n+p\}$	2017
253.	ITVL47	Leveraging Unused Resources for Energy Optimization of FPGA Interconnect	2017
254.	ITVL48	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	2017
255.	ITVL49	Hybrid LUT/Multiplexer FPGA Logic Architectures	2016
256.	ITVL50	FPGA-Based Architecture For A Multisensory Barrier To Enhance Railway Safety	2016
257.	ITVL51	Ultralow-Energy Variation-Aware Design: Adder Architecture Study	2016
258.	ITVL52	Implementation Of AES Using Reversible Cellular Automata Based S-Box	2016
STATIC TIME ANALYSIS			
257.	ITVL53	A Mismatch-Insensitive Skew Compensation Architecture For Clock Synchronization In 3-D ICS	2017

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258.	ITVL54	RSFQ/ERSFQ Cell Library With Improved Circuit Optimization, Timing Verification, And Test Characterization	2017
VLSI WITH MATLAB			
259.	ITVL55	High Performance Integer DCT Architectures For HEVC	2017
260.	ITVL56	A Scalable Approximate DCT Architectures For Efficient HEVC Compliant Video Coding	2017
261.	ITVL57	LUT Optimization For Distributed Arithmetic Based Block Least Mean Square Adaptive Filter	2017
262.	ITVL58	Multiplier less Unity-Gain SDF-FFTS	2017
263.	ITVL59	On Efficient Retiming Of Fixed-Point Circuits	2017
264.	ITVL60	Logic Testing with Test-per-Clock Pattern Loading and Improved Diagnostic Abilities	2017
265.	ITVL61	Input-Based Dynamic Reconfiguration Of Approximate Arithmetic Units for Video Encoding	2016
266.	ITVL62	Floating-Point Butterfly Architecture Based On Binary Signed-Digit Representation	2016
267.	ITVL63	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT	2016
268.	ITVL64	$(4 + 2\log n)\Delta G$ Parallel Prefix Modulo- $(2n - 3)$ Adder via Double Representation of Residues in $[0, 2]$	2016
QCA TECHNOLOGY			
269.	ITVL65	Design of Efficient BCD Adders in Quantum Dot Cellular Automata	2017
270.	ITVL66	Use: A Universal, Scalable, And Efficient	2017

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		clocking Scheme For QCA	
271.	ITVL67	Design Of Adder And Subtract or Circuits In majority Logic-Based Field-Coupled QCA nano computing	2017
DESIGN FOR TESTABILITY			
272.	ITVL68	Design for Testability Support for Launch and Capture Power Reduction in Launch-Off-Shift and Launch-Off-Capture Testing	2017
272.	ITVL69	Low-Power Programmable PRPG With Test Compression Capabilities	2016

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